REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 30 July 2003. Responsive to the rejections made in the Official Action, Claims 1 and 9 have been amended to clarify the combination of methods which form the invention of the subject Patent Application. Additionally, Claims 14 and 15 have been amended to correct informalities therein.

In the Official Action, the Examiner rejected Claims 1-4 and 9-15 under 35 U.S.C. § 103, as being unpatentable over the combination of Andideh, U.S. Patent 6,191,050, Ang, et al., U.S. Patent 6,232,217, and Mei, et al., U.S. Patent 6,475,895.

Before discussing the prior art relied upon by the Examiner, it is believed beneficial to first briefly review the combination of method steps of the invention of the subject Patent Application, as now claimed. The invention of the subject Patent Application is directed to a planarization method of inter-layer dielectrics. The method includes the step of providing a semiconductor substrate including a field oxide, a source, a drain, and a gate formed thereon, or alternately providing a semiconductor substrate having a plurality of metal interconnects formed thereon. The method further includes the step of forming a dielectric layer used as an inter-layer dielectric on the semiconductor substrate. The dielectric layer is formed with a thickness in the range of 3,000 – 15,000 angstroms. Next, the dielectric layer is lapped by

means of chemical mechanical polishing. The method then forms on the lap dielectric layer a cap layer of silicon nitrogen-oxide having a thickness in the range of 300 – 2,000 angstroms and a refractive index of at least 1.6, wherein the cap layer is translucent to ultra-violet light.

It is respectfully submitted that the Andideh reference discloses a method for forming an interlayer dielectric on a semiconductor device. The prior art structure referred to in the Background, relied upon by the Examiner, discloses a semiconductor device 100 formed on a silicon substrate 101 and covered by a phosphosilicate glass layer 103 that is deposited at a thickness of 18,000A and overlaid by an undoped oxide layer 106. As the Examiner admits, the reference does not disclose or suggest forming the cap layer of high refractive index on the lapped dielectric layer. Further, the reference does not recognize the problem solved by the invention of the subject Patent Application and therefore cannot disclose or suggest a solution thereto.

The Ang, et al. reference is directed to a method for forming a metal interconnect within a fluorinated silicon glass dielectric layer. Here, is formed semiconductor structure 10 and planarized by chemical-mechanical polishing. An optional capping layer 20 is then formed over the planarized FSG layer. However, here again, there is no disclosure of the problem solved by the invention of the subject Patent Application, and as the Examiner admits, the reference neither discloses nor suggests the cap layer having a refractive index of

at least 1.6, wherein the cap layer is translucent to ultra-violet light.

The Mei, et al. reference is directed to a semiconductor device structure and process for fabrication wherein a HDP oxide layer fills gaps between the metal structures. Subsequent to the formation of the top surface of the substrate, a first layer 52 of insulating material (high density plasma oxide) 52 is deposited over the metal structure and fills the gaps between such structures. Then, without any planarization, a second insulating layer 56 is deposited over the surface 55 of insulating layer 52. Insulating 56 is a silicon oxynitride layer and it is a "hard surface to provide physical or mechanical protection for the underlying device", column 3, lines 50-52. Thus, the layer 56 is not applied to the layer 52 in order to fill micro scratches generated by the CMP process.

The reference does suggest that the silicon oxynitride film have a refractive index in the range of 1.6 – 1.8 and is transparent to ultra-violet light. However, the reference also suggests that the layer 56 have a thickness which is approximately equal to the thickness of the underlying oxide layer, approximately 800 nm, column 3, lines 64-67.

Thus, none of the references relied upon by the Examiner disclose the problem solved by the invention of the subject Patent Application, and thus their combination cannot be said to form the solution for such a problem.

Arguendo, even if the Mei, et al. reference were combined both with Andideh and Ang, et al., such still would not make obvious invention of the subject Patent Application, as now claimed.

The cap layer of Mei, et al. or incorporated with the combination of Andideh and Ang, et al., such would have to still carry the limitations that the cap layer have the same thickness as the underlying insulating layer. Thus, such combination would not include the step of forming a dielectric layer used as an inter-layer dielectric on the semiconductor substrate, the dielectric layer being formed with a thickness in the range of 3,000 – 15,000 angstroms, and the step of forming on the lap dielectric layer a cap layer of silicon nitrogen-oxide having a thickness in the range of 300 – 2, 000 angstroms and a refractive index of at least 1.6, as now defined in the amended claims. Therefore, the combination of Andideh, Ang, et al. and Mei, et al. cannot make obvious the invention of the subject patent application.

It is now believed that the subject Patent Application has been place in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

David I. Klein
Registration #33,253

Dated: 30 Oct. 2003

Suite 101
3458 Ellicott Center Drive
Ellicott City, MD 21043
(410) 465-6678

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